REMARKS

Reconsideration of this application is respectfully requested in view of the foregoing amendments and the following remarks.

By the foregoing Amendment, claim 1 has been amended. No new matter has been added. Thus, claims 1-8 are pending in this application and subject to examination.

In the Office Action mailed February 28, 2006, claims 1-3 and 8 were rejected under 35 U.S.C. § 102(b) as being anticipated by Mori (U.S. Patent No. 5,949,098). Claims 4-7 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Mori in view of The Applicants' Admitted Prior Art (hereinafter "AAPA"). It is noted that claim 1 has been amended. To the extent the rejections remain applicable to the claims currently pending, the Applicants traverse the rejections, as follows.

Claim 1 Recites Patentable Subject Matter

In rejecting claim 1, the office Action cites to FIG. 3 of Mori, taking the position that Mori discloses each and every feature of the claimed invention. The Applicants respectfully disagree with this characterization of Mori and submit that nothing in the cited prior art, taken alone or in combination, discloses or suggests at least the following combination of limitations of the present invention: (1) "a third power line from which a part corresponding to a position of said bypass capacitor is removed"; and (2) "a fourth power line from which a part corresponding to the position of said bypass capacitor is removed," as recited in amended claim 1. (Emphasis supplied).

Mori is directed to a semiconductor integrated circuit capable of reducing noise, occurring when power is removed from the circuit. As shown in FIG. 3, the semiconductor integrated circuit has a multi-layer structure, including a power wiring layer 310 used for a power conductive line 311, a first insulating layer 320 capable of providing electrical isolation between the power wiring layer 310 and the power/ground wiring layer 330, the first insulating layer 320 having through holes 321 defined therein to enable an electrical connection between the power conductive line 311 and one of power conductive lines 331. The power/ground wiring layer 330 is used for both the power conductive lines 331 to be connected to the power conductive line 311, and for the ground conductive lines 332 to be connected to each of ground conductive lines 352.

The semiconductor integrated circuit shown in FIG. 3 of Mori further includes a second insulating layer 340 capable of electrically providing electrical isolation between the power/ground wiring layer 330 and the ground wiring layer 350, having a through hole 341 defined therein for connecting each of the power conductive lines 331 and a power conductive line 351 to each other, and having through holes 342 defined therein for providing connections between the ground conductive lines 332 and each ground conductive line 352, the ground wiring layer 350 used for the ground conductive lines 352, and having the power conductive line 351 for providing an electrical connection between each of the power conductive lines 331 and the first signal conductive line 371. The semiconductor integrated circuit shown in FIG. 3 of Mori further includes a third insulating layer 360 capable of providing electrical isolation between the ground wiring layer 350 and a signal wiring layer 370, having a through hole 361 defined therein for

connecting the power conductive line 351 and the first signal conductive line 371 to each other and having a through hole 362 defined therein for connecting each of the ground conductive lines 352 and a second signal conductive line 372 to each other, the signal wiring layer 370 used for the signal conductive lines and composed of the first signal conductive line 371, the second signal conductive line 372 and a third signal conductive line 373.

By contrast, as shown in the embodiment of the present invention depicted in FIG. 1, the recited first power line corresponds to reference numeral 2. The recited second power line corresponds to reference numeral 3. The recited third power line corresponds to reference numerals 4a and 4b. The recited fourth power line corresponds to reference numerals 5a and 5b.

As recited in amended claim 1 of the present invention, and shown in the preferred embodiment depicted in FIG. 1, for example, the recited first power line (2) is connected to one terminal of the recited bypass capacitor (1), and the recited second power line (3) is connected to the other terminal of the recited bypass capacitor (1). Therefore, assuming without admitting, that capacitance C32, shown in FIG. 3 of Mori, corresponds to the claimed bypass capacitor, the power/ground wiring layer 330 and the ground wiring layer 350 in FIG. 3 of Mori correspond to the first power line (2) and the second power line (3), as recited in claim 1, as amended.

As further recited in amended claim 1 of the present invention, and as shown in the embodiment of FIG. 1, the recited third power line (4a, 4b) and the recited fourth power line (5a, 5b) are connected to the recited first power line (2) and the recited second power line (3) via the recited first contact (6a, 6b) and the recited second

contact (7a, 7b), respectively, as claimed in claim 1, as amended. Therefore, the structure corresponding to the claimed first power line (2) and the claimed second power line (3), disclosed in FIG. 3 of Mori, *i.e.*, the power/ground wiring layer 330 and the ground wiring layer 350, should be connected to a third power line and a fourth power line via contacts. Thus, the Mori power wiring layer 310 and signal wiring layer 370 correspond to the third power line (4a, 4b) and the fourth power line (5a, 5b), as recited in claim 1.

As claimed in claim 1 of the present invention, and as shown in the embodiment depicted in FIG. 1, for example, a part corresponding to the position of the bypass capacitor is removed from the third power line (4a, 4b) the fourth power line (5a, 5b). However, no part corresponding to capacitance C32 is removed from power wiring layer 310 and signal wiring layer 370 of Mori.

Similarly, assuming without admitting, that capacitance C33, shown in FIG. 3 of Mori, corresponds to the claimed bypass capacitor, the power/ground wiring layer 330 on both sides of capacitance C33 in FIG. 3 of Mori correspond to the first power line (2) and the second power line (3), as recited in claim 1, as amended. The Mori power wiring layer 310 and ground power layer 350 correspond to the third power line (4a, 4b) and the fourth power line (5a, 5b), recited in claim 1 and shown in the embodiment of FIG. 1 of the present invention. Again, no part corresponding to capacitance C33 is removed from power wiring layer 310 and ground power layer 350 of Mori.

For at least these reasons, the Applicants respectfully submit that claim 1 is allowable over the cited art.

Claims 2-8 Recite Patentable Subject Matter

Regarding claims 2-8, the Applicants respectfully submit that each of these claims depends from allowable claim 1, and is therefore allowable for at least the same reasons.

Conclusion

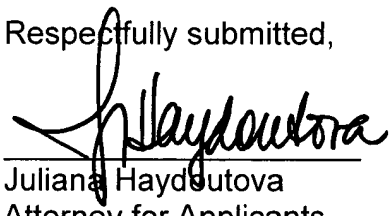
For all of the above reasons, it is respectfully submitted that the claims now pending patentably distinguish the present invention from the cited references. Accordingly, reconsideration and withdrawal of the outstanding rejections and an issuance of a Notice of Allowance are earnestly solicited.

Should the Examiner determine that any further action is necessary to place this application into better form, the Examiner is encouraged to telephone the undersigned representative at the number listed below.

In the event this paper is not considered to be timely filed, the Applicant hereby petitions for an appropriate extension of time. The Commissioner is hereby authorized to charge any fee deficiency or credit any overpayment associated with this

communication to Deposit Account No. 01-2300, referring to client-matter number 107337-00058.

Respectfully submitted,



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